



## **Quality and Reliability Report**

**Product quality and reliability have always been significant factors at VITE.**

### **Introduction**

This VITE Quality and Reliability Report is intended to provide customers with an overview of VITE's product quality and reliability method. VITE is a quality leader in crystal-based frequency control products (FCP). Our leadership position results from our end-to-end quality processes that fully meets or exceeds customer expectations. Product quality and reliability have always been significant factors at VITE, which are built into the product right from inception. The new competitive environment in the communications industry and other sectors of the consumer electronics market, present VITE with the challenge of maintaining our reputation for product quality and reliability while producing products at competitive prices. To achieve this goal, VITE has focused on strict adherence to quality and reliability standards and practices.

### **Qualification Tests**

The qualification of VITE's frequency control products entails a variety of environmental and life tests. These tests are based on widely accepted industry standards, such as the military MIL-STD-883, ASTM, IEC, and BELLCORE (TR-NWT-357). When required by application or by customer, new tests or modified versions of standard tests are also used. Tests commonly used in the qualification of the frequency control products are described below.

#### **Assembly Pre-conditioning (APC)**

The purpose of this test is to evaluate the effect of board assembly processes on components. Exposure to thermal operations during soldering as well as to chemicals during post-reflow cleaning can potentially affect the reliability of the product. A complete simulation requires more than one thermal exposure to duplicate board assembly as well as any potential subsequent repair operations. Typically three simulations are done by using IR reflow, convection reflow, vapor-phase soldering or wave soldering depending on the type of the component. For frequency control products that are hermetically sealed the AP test is useful in establishing parametric changes resulting from the board assembly process. Simulations to cleaning processes such as exposure to flux, DI water and detergents may not be required when product is hermetically sealed. The AP test may also include thermal cycling to simulate the transportation/storage environment the product may encounter prior to actual assembly.

#### **Bond Strength Test (BDS)**

This test is intended for verifying that all bonds and attachments (e.g. thermo compression bonds, die attach bonds, wire bonds and applique solder joints) conform to design specifications. These tests include wire bond pull and shear, die shear, beam-lead bond strength, and solder joint strength. The test requirement is per MIL-STD-883, and applicable design specifications or process drawings.

#### **Electrical Characterization Test (EC)**

This test is performed on each individual component code. Functional behavior and important parametric characteristics are examined at room temperature and at specified operating temperature extremes to confirm that the product meets its design specifications such as in the

design specifications or to advertised data-sheet requirements. Important electrical parameters are recorded for each sample, and measured parameter distributions are compared to the specification limits. This is a non-destructive test.

#### **Electrical Discharge Test (ESD)**

This test assesses the susceptibility of individual codes to damage from discharges of static electricity. The procedure includes tests using both a human-body model and a charged device model per the Lucent X-19435 test method. This is a destructive test.

#### **High Temperature Aging (HTA)**

The HTA test is used for devices that may fail from thermally activated parametric degradation over time. Crystal-based frequency control devices with bulk acoustic wave crystal resonators (e.g. oscillators), and surface acoustic wave filters (e.g. SAW filters) are examples of devices that can exhibit drift of electrical parameters with time. In this test, devices are aged with bias (those with active IC devices) or without bias at elevated temperatures and the drifts in device's parameters are measured periodically over time.

The test is performed at one or more aging temperatures (such as 85°C, 100°C, 125°C, 150°C, or other temperatures depending on the device characteristics) for a minimum of 1000 hours with several measurements over this duration as specified in the qualification plan. When devices are aged under bias, they are cooled under bias after removing from the chamber for testing. Test can be extended beyond 1000 hours for information. The average parametric drift, linear over log-time, is extrapolated to estimate the end-of-life drift and used to estimate aging under typical use conditions.

#### **Internal Moisture Test (IM)**

The purpose of this test is to measure the water vapor contents of hermetically sealed modules. Excessive moisture levels coupled with ionics (such as from process chemicals, organic adhesives etc.) inside the package enclosures can potentially results in corrosion type failures over time. This is a destructive test, and is performed per MIL-STD-883. The specified moisture level is 5000 ppmv of water vapor. Long-term reliability studies for some FCP modules (such as ceramic oscillators) with moisture levels exceeding this threshold have not shown any adverse impact on product reliability from the water vapor. Therefore method 1018 requirements are currently used as an objective, and the IM test is performed for information only unless required by customer application.

#### **Internal Visual (IV)**

The purpose of this test is to assess visual quality of unencapsulated or unsealed modules. The test is performed per MIL-STD-883, method 2017 or per applicable design/manufacturing documentation requirements. Among attributes that are visually inspected are die attach coverage, wire bond quality defects in package or in the internal components, contamination, and general workmanship.

#### **Lead Integrity Test (LI)**

This test is performed on the external leads of the module and is intended to assess the strength of the lead/module connections. This destructive test is performed per MIL-STD-883, method 2025, and can include lead pull, lead bending as well as lead fatigue tests.

#### **Mechanical Sequence Test (MS)**

This destructive test is intended to assess the mechanical robustness of the module to mechanical forces such as during handling and transportation. The test sequence consists of variable frequency vibration per MIL-STD-883, method 2007 and mechanical shock per method 2002. Test conditions commonly used are test A (20-g peak acceleration) or test B (50-g peak acceleration) for vibration, and either test A (500-g) or test B (1500-g) for the mechanical shock depending on the inherent capability of the product to withstand the severity of the stress level. Most FCP products are tested to the lower test A conditions. Ceramic packaged products have shown capability to survive higher shock levels, such as Test B condition for shock.

**Physical Dimensions Test (PD)**

The purpose of this test, performed in accordance with MIL-STD-883, method 2016, is to check compliance of the physical outline to design specifications. Critical external dimensions of the module, such as lead length and coplanarity are measured to verify design specifications. This is a non-destructive test.

**Solderability Test (SLD)**

The purpose of this test is to ensure component lead solderability during the board assembly process. This test can be performed per MIL-STD-883, method 2003, or per the wetting balance test. The test can be performed with or without steam aging, depending on customer requirements. Steam aging is intended to simulate the effect of component storage on lead solderability prior to board assembly. This is typically a non-destructive test.

**Temperature Cycling Test (TC)**

This test applies thermally induced stress to accelerate material fatigue and precipitate failures associated with thermal mismatches. This test is also used as a screen to remove devices with poorly bonded devices or applique components. Temperature cycling consists of subjecting the modules to repeated excursions between hot and cold thermal extremes. Typical cycling regimes are 300 cycles, -55°C to 125°C for FCP devices which is frequently extended to 500 cycles for information. Customer requirements may also define other cycling conditions. This test is considered non-destructive when used in a short-duration test such as for screening or in reliability monitoring programs. Extended cycling, such as for qualification or re-qualification is considered destructive. The qualification test acceptance criterion is based on meeting end-of-life requirements after the completion of cycling.

**Thermal Shock (TS)**

This test is intended to induce the same types of failure as from temperature cycling. Unlike TC which is performed using air as a transfer medium in the test chamber, TS is a liquid-to-liquid transfer test. TS can therefore generate significantly higher thermal transfer rates. TS is performed if required by application only, and can be done in sequence with the normal temperature cycling test.

**Thermal Step Stress Aging (TSS)**

This test is performed on frequency control modules to evaluate long-term parametric drift in a shorter duration than that required for High Temperature Aging performed under isothermal conditions. In this test, the test sample is thermally aged for a fixed interval at successively higher thermal steps. Typical regimen is 16 hours from 80°C to 220°C (based on module capability). The modules are electrically tested at the end of each step and returned to the aging chamber at the next higher temperature. The parametric drift trend over the temperature range is compared to a group of control modules to assess any variations in the aging behavior as a result of the process change under study. Although the actual aging under isothermal HTA conditions cannot be readily predicted using step stress aging results, generally the test captures the expected end-of-life drift in a relatively short duration. The test therefore can be used for assessment of potential long-term aging drifts, and acceptance criteria are as defined in the qualification plan.

Test	Test Conditions	Comments
<b>BDS</b> (Bond Strength)	Per MIL-STD-883	Wirebond pull strength; sample represents total bonds from a minimum of 5 modules
	Per MIL-STD-883	Die shear strength, 5 modules
<b>EC</b> (Electrical Characterization)	Functional Electrical Test	Electrical Tests to verify conformance to design requirements. Tests performed at ambient conditions, and over operating temperature range
<b>ESD</b>	Per Lucent X-19435	Minimum requirement of 500v for all pins for modules operating at <200 MHz
<b>HTA</b> (High Temperature Aging)	T = 85°C, 100°C, 125°C Duration: 1000 hours	Modules with active ICs are aged under specified bias. Modules aged at one or more temperatures with several measurements over the aging duration.
<b>IM</b> (Internal moisture)	Per MIL-STD-883	Residual gas analysis for internal water vapor. Test performed for information only.
<b>LI</b> (Lead Integrity)	Per MIL-STD-883	Sample represents total number of leads from a minimum of 5 modules for each test (pull, bend and fatigue)
<b>MS</b> (Mechanical Sequence Shock and Vibration)	Per MIL-STD-883 Shock per M2002, Test A or B Vibration per M2007, Test A or B	FCP are tested to Test A for vibration, and either Test A or B for shock. Acceptance based on functional test and leak test after completion of test.
<b>PD</b> (Physical Dimensions)	Per MIL-STD-883	Critical outline dimensions and coplanarity measured for design conformance
<b>SLD</b> (Solderability)	Per MIL-STD-883	Sample represents total number of leads from a minimum of 5 modules.
<b>TC</b> (Temperature Cycling)	Tmin= -55°C Tmax= 125°C N = 300 cycles	Acceptance based on EOL criteria and passing leak test after the completion of cycling.
<b>TS</b> (Thermal Shock)	Per MIL-STD-883	Test performed if required by customer application. Acceptance based on EOL criteria and passing leak test.
<b>TSS</b> (Thermal Step Stress)	80°C to 220°C with 16 hours of aging at each successive thermal step	Test used for characterizing parametric aging over the thermal step profile to compare baseline aging (in the control group) with that in the test sample group from process changes under study. Acceptance criteria as defined in the qualification plan.

## Reliability Monitoring

Reliability monitors are performed on samples from representative codes of a specific component (product family) class. The reliability monitor tests are short-term, non-destructive accelerated life tests and function as early warning tests that highlight possible design or process problems. They can be viewed as a process check on the product reliability, and provide assurance that the manufacturing processes are within their normal process limits and therefore the product reliability is consistent with expected norm as established during initial product qualification. Reliability monitoring tests thus are performed on components in an ongoing quality assurance program.

Reliability monitoring tests in place for the FCP products include: short-duration accelerated life test and temperature cycling. These tests are performed on a sample basis periodically (quarterly) on representative codes from the standard product families.

### **Re-qualification**

The re-qualification program uses some of the tests performed in the qualification program. Sample sizes and intervals are generally in compliance with industry standards such as the BELLCORE TR-NWT-357, "Generic Requirements for Components Used in Telecommunications Equipment", and MIL-STD-883. Typically re-qualification interval is three years. Major products changes that can potentially affect the product reliability, however, are re-qualified as required, to assure that the change does not adversely affect product reliability. Customer notification and approval prior to implementation of design/process changes is submitted to customer for re-qualification.

### **Incoming Material Quality Control**

The intent of this program is to ensure that only product that meets VITE specifications is procured. Appropriate control over sub-contractors includes a documentation procedure for supplier evaluation and selection, and requirement from vendors for shipment of quality data with each shipped lot conformance to VITE specifications is periodically checked by incoming quality inspection of critical materials. Additionally, the performance of key suppliers is monitored by requirements for quality system maintenance, process control over significant manufacturing operations, and periodic facility audits to VITE's requirements.

### **Product Family Failure Rates (FITs)**

A long-term steady-state failure rates is often required by circuit and system engineers for allocations of the failure rates (FITs) at the component level during circuit pack and system designs. A "FIT", which stands for failure in time, is a widely used term to describe failure rates of electronic components, and as used here, represents number of failure in  $10^9$  or billion hours of operation. Other measures such as % fail or failures in 1000 hours are also used. FIT rates for crystals and oscillators in the 50-100 FIT ranges are reported.

VITE failure rates from life test data represents cumulative results from many life test studies conducted over the several years of life history of these products since first introduced into manufacture. Such data not only represents initial design qualification results but also subsequent studies undertaken with the intent of qualifying changes to the products after manufacturing introduction. Such qualification are often required when changes to process or materials are made as an ongoing effort to improve the product quality, and manufacturing yields in order to reduce costs to remain competitive in the market. Life test data was translated to the lower temperature use conditions by means of the Arrhenius acceleration factor using activation energy of 0.5 eV. This was selected conservatively based on observations of parametric aging over different accelerated temperature stress levels, from 85C to 150C.

### **Mean Time Between Failure (MTBF)**

Another way to express failure rates is by "mean time between failures" (MTBF). Failure rates expressed in this fashion serve a useful purpose for system maintenance engineers who need to plan for warranty expenses, replacement costs, stocking costs for spares and inventory, or otherwise need to develop a strategy for system repair & maintenance management. Although the MTBF can be shown to be related to the actual failure rates, knowledge of the failure rate model is required for an exact conversion between the failure rate in FIT and the MTBF. However, the inverse of the FIT value can be used as the MTBF, which is valid for dealing with constant steady state failure rates of electronic components that typically tend to follow the exponential distributions which yield constant failure rates.

### **Reference:**

1. Quality & Reliability Report, Dr. Ram Avikar, Vectron International