

CD-700...A Quartz Stabilized PLL

THE NEW COMPLETE PLL SOLUTION

... to 65 Mb/s

A Phase-Locked Loop ASIC

... with a Quartz Stabilized VCXO

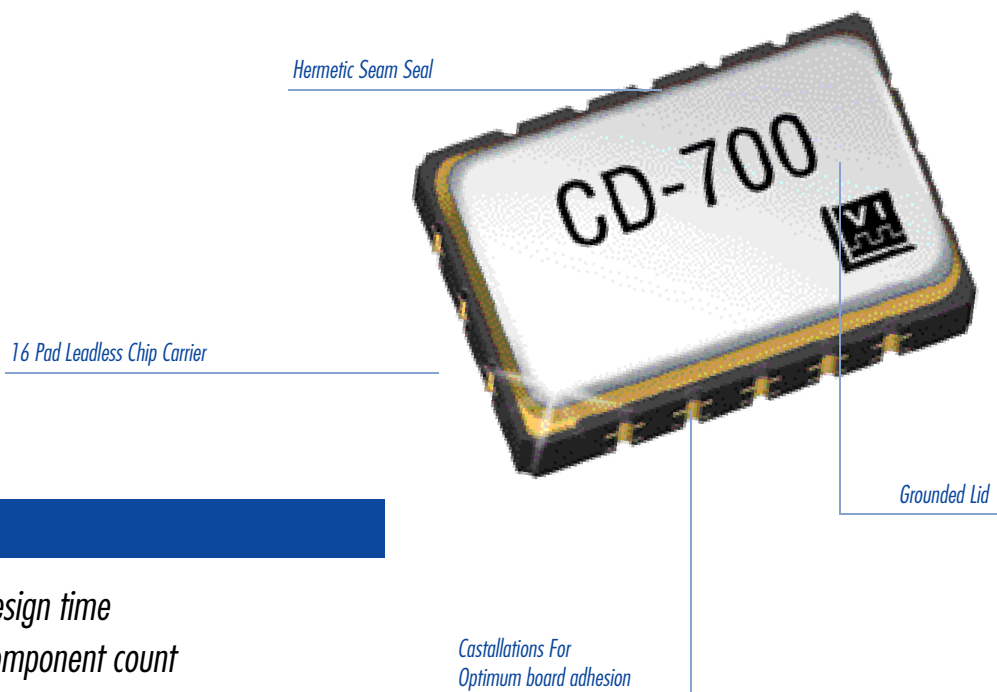
THREE APPLICATIONS:



CD-700

Flexible Modular Solution A Quartz Stabilized PLL

It's a phase-locked loop ASIC with a quartz stabilized VCXO!



It will:

- *Reduce: design time
component count
board space*
- *Improve: jitter performance
reliability*

It performs:

- *Clock Recovery & Data Retiming*
- *Frequency Translation*
- *Clock Smoothing*
- *Clock Switching*

In applications up to 65.536 Mb/s:

- *ATM, SONET/SDH, DWDM*
- *xDSL, Network Communications*
- *Digital Audio/Video, PBX Systems*

What Does It Do?

Vectron International's CD-700 is a user-configured, phase-locked loop (PLL) solution designed to simplify a wide variety of clock recovery and data retiming, frequency translation, clock smoothing and clock switching applications. The device features a phase-lock loop ASIC with a quartz stabilized VCXO for superior stability and jitter performance. This highly integrated module provides unsurpassed performance, reliability and quality. The proprietary ASIC device includes a refined Phase Detector, a Loop Filter Op-Amp, a Loss of Signal Alarm with Clock Return to Nominal feature, a VCXO circuit, and an optional 2ⁿ divided output.

The ASIC and quartz resonator are housed in a hermetic 16-pad ceramic leadless chip carrier. The VCXO frequency (OUT1) and division factor (OUT2) are factory set in accordance with customer specifications. PLL response is optimized for each application by the selection of external passive components. Software is available from Vectron to aid in loop filter component selection and loop response modeling.

Features:

PLL with quartz stabilized VCXO

Output jitter less than 20 ps

Loss of signal (LOS) alarm

Return to nominal clock upon LOS

Input data rates from 8 kb/s to 65.536 Mb/s

Surface mount option

Tri-state output

User defined PLL loop response

NRZ data compatible

Robust hermetic ceramic package

Single +5.0 V or +3.3V supply

Benefits:

Flexible modular solution

Reduce design time

Increase circuit reliability

Less board space

Reduces component count

What is the main benefit of the CD-700?

It's a single drop-in Quartz Stabilized PLL solution.

What's Inside?

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- For input RZ data, Manchester encoded data, and input clock recovery applications, the output clock must run at two times the input rate to ensure that the input is clocked correctly. Since the output clock has a maximum frequency of 65.536 MHz, these inputs are limited to a maximum rate of 32.768 MHz.
- OUT2 is a binary submultiple of OUT1, or it may be disabled.
- A 0.01 μ F and 0.1 parallel capacitor should be located as close to pin 14 (and grounded) as possible
- Figure 1 defines these parameters. Figure 2 illustrates the equivalent five gate TTL load and operating conditions under which these parameters are tested and specified. Loads greater than 15 pF will adversely effect rise/fall time as well as symmetry.
- A loss of signal (LOS) indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.
- Symmetry is defined as (ON TIME/PERIOD with $V_s=1.4$ V for both 5.0 V and 3.3 V operation.

Parameter	Symbol	Min	Typical	Max	Unit
Output Frequency (ordering option) ^{1,2}					
Out 1, 5.0 V option	f_o	12.000		65.537	MHz
Out 1, 3.3 V Option	V_{DD}	12.000		51.840	MHz
Supply Voltage ³					
+5.0	V_{DD}	4.5	5.0	5.5	V
+3.3		2.97	3.3	3.63	V
Supply Current					
	I_{DD}			63	mA
Output Transition Times:					
Rinse Time ⁴	t_R			5	ns
Fall Time ⁴	t_F			5	ns
Input Logic Levels:					
Output Logic High ⁴	V_{OH}	2.0			V
Output Logic Low ⁴	V_{OL}			0.5	V
Loss of Signal Indicator					
Output Logic High ⁴	V_{OH}	2.5			V
Output Logic Low ⁴	V_{OL}			0.5	V
Nominal Frequency on Loss of Signal ⁵					
Output 1				± 75	ppm
Output 2				± 75	ppm
Symmetry or Duty Cycle ⁶					
Out 1	SYM1			40/60	%
Out 2	SYM2			45/55	%
RCLK	RCLK			40/60	%
Absolute Pull Range (ordering option) over operating temp, aging, power supply variations					
	APR	± 50			ppm
		± 80			
		± 100			
Test Conditions for APR (+5.0 V option)					
	V_c	0.5		4.5	V
Test Conditions for APR (+3.3 V option)					
	V_c	0.3		3.0	V
Gain Transfer					
				Positive	
Phase Detector Gain					
+5V option			0.53		rad/V
+3.3V option			0.35		rad/V
Operating temperature (ordering option)					
			0/70 or -40/85		$^{\circ}$ C
Control Voltage Leakage Current					
	I_{VCO}			± 1	μ A

Table 1.

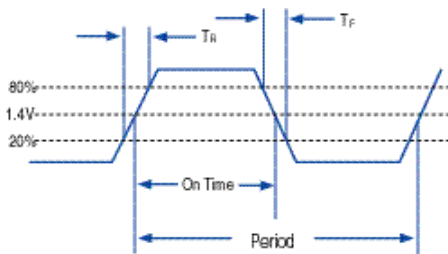


Figure 1.

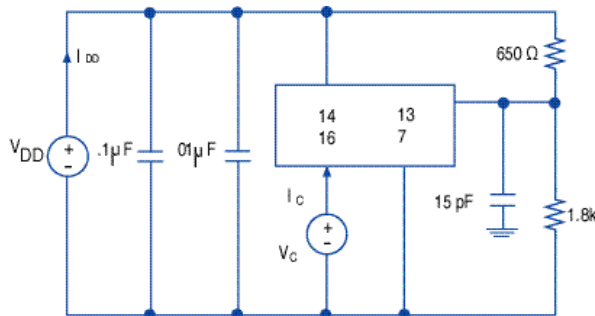


Figure 2.

Pin	Symbol	Function
1	OPOUT	Output terminal of internal operational amplifier.
2	OPN	Negative input terminal to internal operational amplifier.
3	PHO	Output signal produced by phase detector.
4	LOSIN	With LOSIN set to a logic high, the external input to the VCXO (VC) is disabled and the VCXO returns to its nominal center frequency. With LOSIN set to logic low, the external input to the VCXO is enabled. The LOSIN input has an internal pull-down resistor.
5	DATAIN	Input data stream to phase detector (TTL switching thresholds).
6	CLKIN	Input clock signal to phase detector (TTL switching thresholds).
7	GND	Circuit and cover ground.
8	LOS	Loss of signal indicator is set to a logic high if no transitions are detected at DATAIN after 256 clock cycles. As soon as a transition occurs at DATAIN, LOS is set to a logic low.
9	RCLK	TTL compatible recovered clock.
10	RDATA	TTL compatible recovered clock.
11	OUT2	Divided version of internal VCXO output clock (TTL).
12	HIZ	When set to a logic low, output pins OUT1, OUT2, RCLK, and RDATA buffers are set to high-impedance state. When set to a logic high or no connect, the device functions and output pins OUT1, OUT2, RCLK, and RDATA are active. This input has an internal pull-up resistor.
13	OUT1	Output clock of internal VCXO (TTL).
14	V _{DD}	+5.0 V or +3.3 V
15	OPP	Positive input terminal to internal operational amplifier.
16	V _C	Control voltage input to internal voltage controlled crystal oscillator (VCXO).

Table 2.

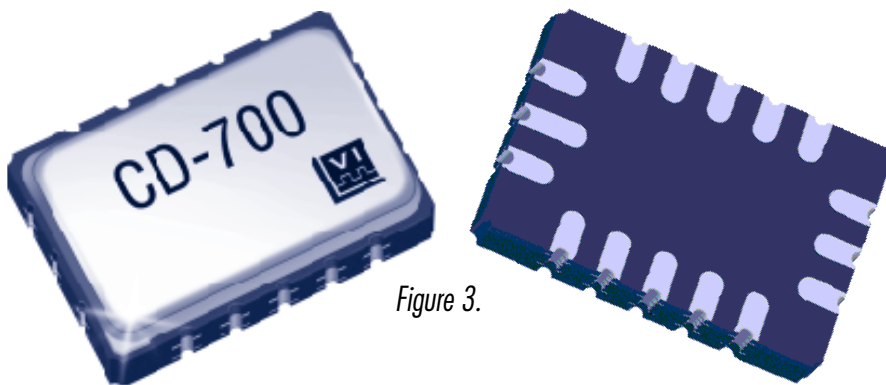


Figure 3.

Why would someone buy a CD-700?

To save design time, reduce component count, conserve board space, and optimize manufacturing efficiency.

How Is It Built?

The CD-700 is a user-configured phase-locked loop (PLL) integrated circuit. It includes a voltage controlled crystal oscillator (VCXO), an operational amplifier, a phase detector, and additional integrated functions for use in digital synchronization applications. These applications include timing recovery and data pulse restoration for data signals, clock frequency translation and smoothing, synchronous distributed clock networks, and clock frequency synthesis.

What is the output of the phase detector?

The CD-700 phase detector output is a DC signal, under locked conditions, and is nominally 2.1 Volts. The phase error (which is typically a pulse for digital phase detectors) is converted to a DC level, making it easy to design the loop filter.

How long does the CD-700 take to detect a loss of signal?

If there are no transitions on DATAIN for a period of 256 clock cycles, LOS is set to a logic 1. LOS is reset to logic 0 as soon as there are DATAIN transitions.

CD-700 Elements

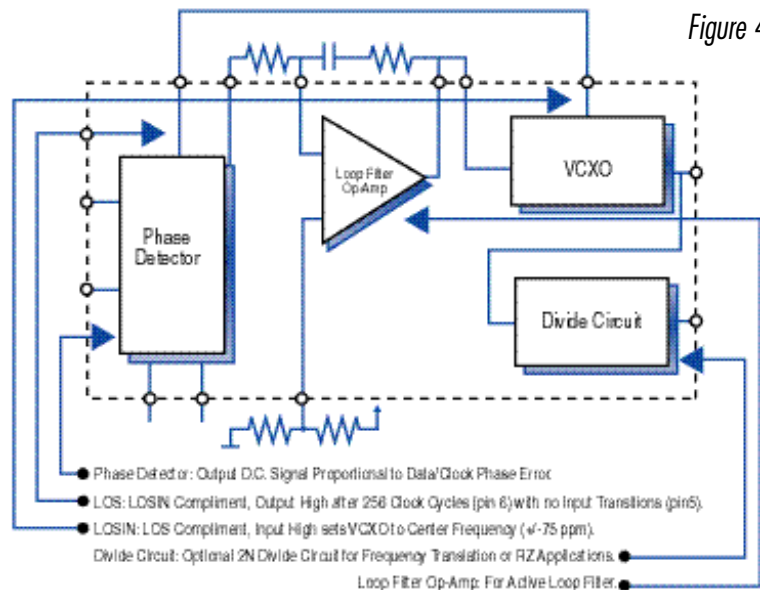


Figure 4.

Phase Detector

The phase detector is designed to accept an NRZ data stream at DATAIN (Pin 5- refer to Figure 5), but may be used for clock signals and other data types. The input buffers are designed to switch at a TTL switching threshold of 1.4 V.

The phase detector's inputs are:

- DATAIN (Pin 5) - the input clock or NRZ data signal
- CLKIN (Pin 6) - the clock signal feedback from the VCXO output OUT1 or OUT2

And the outputs are:

- RCLK (Pin 9) - the regenerated clock signal
- RDATA (Pin 10) - the retimed data signal
- PHO (Pin 3) - the phase detector output
- LOS (Pin 8) - a loss of signal detector

The phase relationship between the regenerated clock signal, RCLK (Pin 9), and the regenerated data signal, RDATA (Pin 10), is shown in Figure 6.

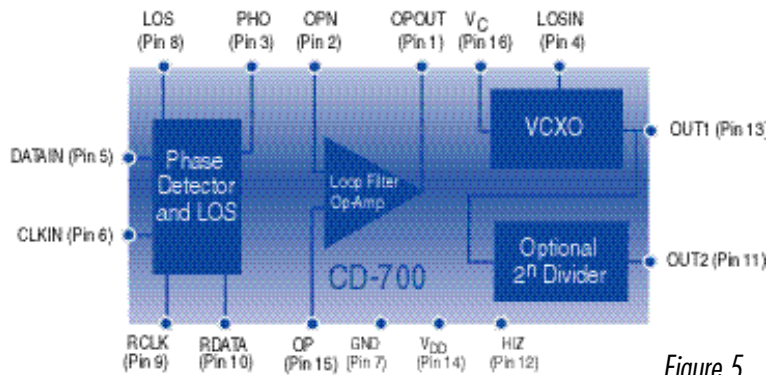


Figure 5.

The falling edge of RCLK is coincident with the center of the regenerated NRZ RDATA pulse. Figure 6 shows a 1010 data stream with a 100% data transition density. In general, this will not be the case and input data will have fewer data transitions. However, the phase detector will still seek to align the falling edge of the RCLK signal with the center of each RDATA pulse.

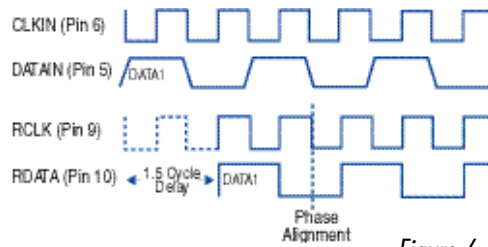


Figure 6.

For applications where the input clock or data signal, DATAIN, is very low in frequency (<200kHz), clock information may pass through the phase detector because of its finite low pass characteristic. In applications such as this, an additional pole may be necessary in the loop filter to attenuate these AC components prior to the VCXO input. Please contact Vectron's Applications Engineering staff for further detail.

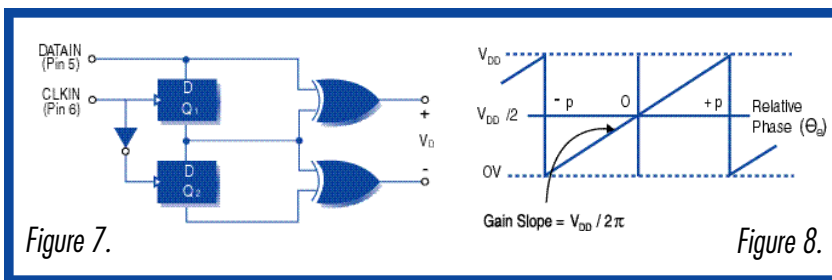


Figure 7.

Figure 8.

Phase Detector Gain Calculation

The schematic diagram (figure 7) shows a simplified representation of the phase detector's basic error generation function. The actual circuit is more complex and includes circuitry to reduce the CD-700's dependence on input data duty-cycle. In general, the CD-700 is insensitive to duty cycle and duty cycle changes. This circuit provides a output (V_D) DC level which is proportional to the relative phase of DATAIN (Pin 5) and CLKIN (Pin 6). A plot of the output (V_D) versus relative phase (Θ_e) is shown in Figure 8. The slope of the output (V_D) versus relative phase (Θ_e) is $V_{DD}/2$.

The phase detector block also includes an output gain stage which should be considered when calculating the gain of the complete phase detector block. This gain stage has a gain of $2/3$, and converts the differential signal to a single-ended DC output.

*How is it
manufactured?*

*The CD-700 is
assembled in
"state of the art"
class 100 and class
10,000 clean
rooms using leading
edge, high volume
automation equip-
ment and advanced
ASIC technology.*

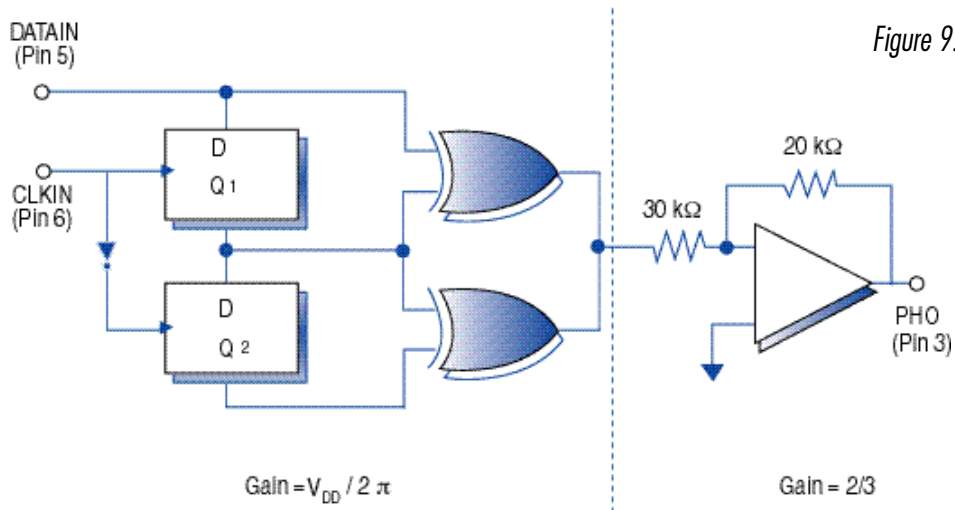


Figure 9.

Phase Detector Gain = $[V_{DD}/2]$ * $[2/3]$ * $D = 0.53 * D$ for 5 Volt and $0.35 * D$ for 3.3 Volt Supply
 Where D = input data transition density. For example $D = 1$ for 100% transition density (e.g., clock signal)
 and $D = 0.5$ for 50% transition density (e.g., balanced NRZ data).

LOS and LOSIN

The LOS circuit provides an output alarm flag when the DATAIN input signal is lost. The LOS output is set “logic high” after 256 consecutive CLKIN periods with no DATAIN transitions. This signal can then be used to either flag external alarm circuits and/or drive the CD-700’s LOSIN circuit. When the LOSIN input is set “logic high,” the loop filter op-amp output is set mid supply to facilitate fast lockup when DATAIN is restored. In addition, the VCXO control voltage is internally set to hold the VCXO at its nominal frequency (± 75 ppm). When LOSIN is low or has no connection, the VCXO’s control voltage input is enabled (LOSIN has an internal pull-down resistor).

Loop Filter

Although various loop filter configurations may be considered, most CD-700 applications use the basic integrator filter of Figure 10. This type of filter provides high DC gain to ensure proper clock and data alignment. The ratio of $R1$ to RF sets midband gain and can be used to adjust the loop bandwidth. The loop filter is usually designed to be 100ppm times the input frequency and should have a high damping factor to minimize peaking. The reference for the non-inverting input is set at midsupply by $R2$ and $R3$. Software is available to help in the selection of $R1$, CF and RF .

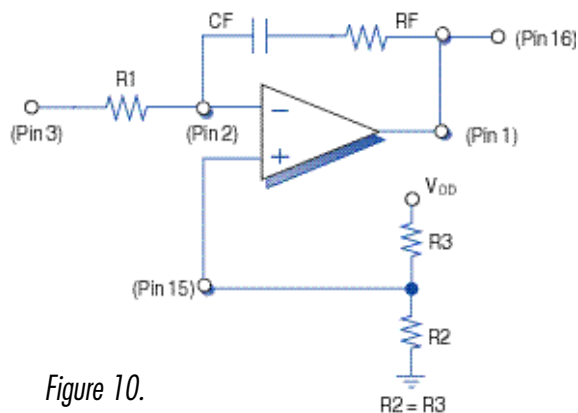


Figure 10.

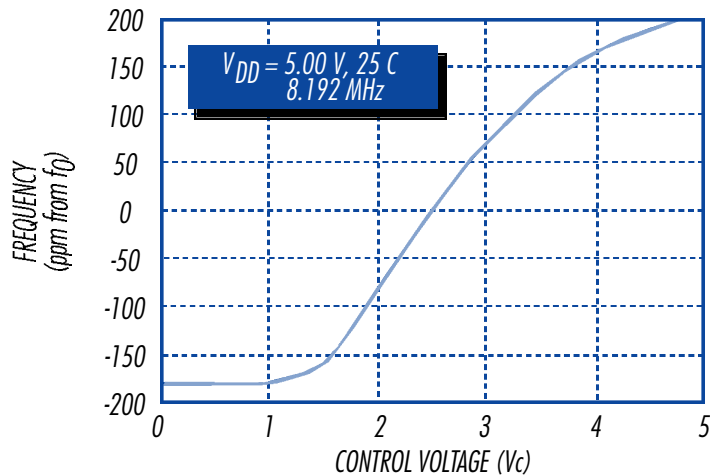


Figure 11.

CD-700 VCXO Frequency Deviation vs. Control Voltage

VCXO

The CD-700's VCXO is a varactor-tuned crystal oscillator which produces an output frequency controlled by a control voltage, V_c . The tracking range of the VCXO is specified as absolute pull range (APR) when ordered. An APR of ± 50 ppm guarantees that the CD-700 can track an input source frequency with ± 50 ppm stability over all operating conditions, including temperature, time, power supply and load variations. A typical frequency versus V_c curve for the VCXO in the CD-700 is shown in figure 11. When designing PLLs, the VCXO gain is an important parameter. As a rule of thumb, the frequency deviation for the CD-700 VCXO is 100 ppm/V.

For example, a 10 MHz VCXO has an average gain of 1000 Hz/V. The peak value of kV is about twice this value at approximately 2.5 V, and one half this value at 1 V and 4 V.

For many loop calculations, the gain is expressed in rad/Vs which would be $2 \times (100 \text{ ppm} * f_0/\text{Vs})$ for the previous example.

Oscillator Aging

Any crystal-stabilized oscillator typically exhibits a small shift in output frequency during aging. The major factors which lead to this shift are changes in the mechanical stress on the crystal and mass-loading of foreign material on the crystal.

As the oscillator ages, relaxation of the crystal mounting stress or transfer of environmental stress through the package to the crystal mounting arrangement can lead to frequency variations. Vectron has minimized these two effects through the use of a miniature AT-cut strip resonator crystal which allows a superior mounting arrangement and results in minimal relaxation and almost negligible environmental stress transfer.

How is quality assured?

In addition to extensive testing, the basic design consists of a few highly engineered, robust components; quality is further assured by advanced ceramic packaging and fully automated assembly.

Mass-loading on the crystal generally results in a frequency decrease and is typically due to out-gassing of material within a hermetic package or from contamination by external material in a non-hermetic package. Vectron has minimized the impact of mass loading by ensuring hermetic integrity and minimizing out-gassing by limiting the number of internal components through the use of ASIC technology.

Under normal operating conditions with an operating temperature of 40°C, the CD-700 will typically exhibit 2 ppm aging in the first year of operation. The device will then exhibit 1 ppm aging the following year with a logarithmic decline each year thereafter.

I'm not familiar with APR. Could you explain it in more detail?

APR is the guaranteed frequency error (in ppm) the VCXO can track. This takes the guesswork out of the total pull range which drifts and is affected by temperature, aging, power supply etc.

What's the difference between OUT1 and OUT2?

OUT1 is the direct output from the VCXO and is limited to frequencies in the 12 MHz to 65 MHz range. OUT2 is an optional 2ⁿ divided VCXO output. The divide ratio is factory set at 2, 4, 8, ... or 2ⁿ, up to 256.

Absolute Pull Range

Absolute pull range (APR) is specified by the fourth character of the product code (see figure 26). APR is the minimum guaranteed frequency shift from f_0 over variations in temperature, aging, power supply and load. Both frequency and environment limit the specified APR. The total pull range for the VCXO contained in the CD-700 is typically between 200 ppm and 400 ppm. A 50 ppm APR CD-700 fully tracks a 50 ppm source oscillator or any other 50 ppm reference over the operating temperature range, life of the product, power supply and measurement variations.

Output Divider Circuit

An internal 2ⁿ divided output is available at OUT2. The value of n varies from 1 to 8 and is set during manufacture. This provides divide ratios from 2 to 256. A "no output" option may also be selected to minimize power usage and jitter.

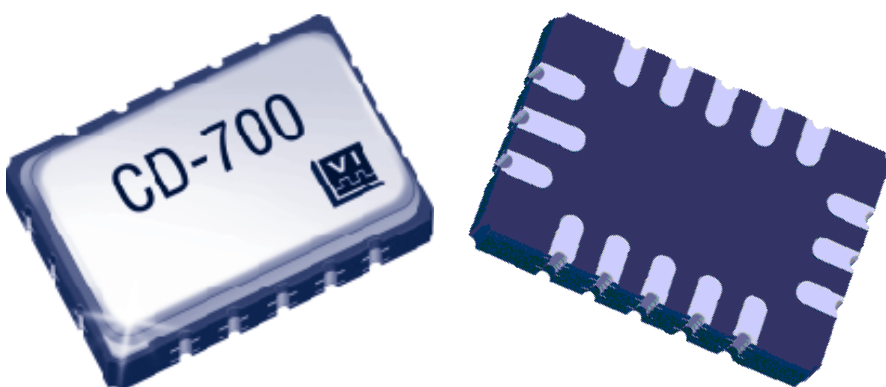
Divider Note: *The frequency of OUT1 is the fundamental frequency of the VCXO used in the CD-700. The lowest frequency VCXO (OUT1) available in the CD-700 is 12 MHz, and the highest frequency is 65.536 MHz. Therefore, the frequency range of OUT1 is between 12 MHz and 65.536 MHz. Since OUT2 is a division of OUT1 and can vary from $OUT1 \div 2$ to $OUT1 \div 256$, OUT2 ranges from 46.875 kHz ($12 \text{ MHz} \div 256$) to 32.768 MHz ($65.536 \text{ MHz} \div 2$). Lower frequency inputs may be supplied to the phase detector of the CD-700, but an external divider in the feedback loop is required. With an external divider in the feedback loop, clock and data signals down to 8 kHz can be used as phase detector inputs.*

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Vectron employs a Human Body Model (HBM) and a Charged Device Model (CDM) for ESD susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used to define the mode.

MODEL	ESD Threshold, Minimum	Conditions
Charged Device	1000 V	JESD22-C101
Human Body	1500 V	MIL-STD 883, Method 3015

Table 3.



How is it packaged?

The CD-700 is a very robust product which is assembled on an automated manufacturing line. It is packaged in a 16-pad ceramic with a seam-welded step lid, hermetically sealed for long term reliability. Options include APR and an extended temperature range. Tape and reel packaging will be used for production orders.

How Does It Perform?

A typical PLL is illustrated in Figure 12. Be advised that many textbook equations describing loop dynamics, such as capture range or lock-in time, are based on ideal systems. Such equations may not be accurate for real systems with nonlinearities, DC offsets and noise. A PLL is a feedback system which forces the output frequency to lock-in both phase and frequency to the fundamental frequency of the input signal.

When initially out of lock, the output of the phase detector is proportional to the difference in frequency between the two phase detector inputs. This beat note varies the output frequency of the VCXO, and in a properly designed phase-locked loop, the loop action forces V_C to the correct value to bring the system into lock.

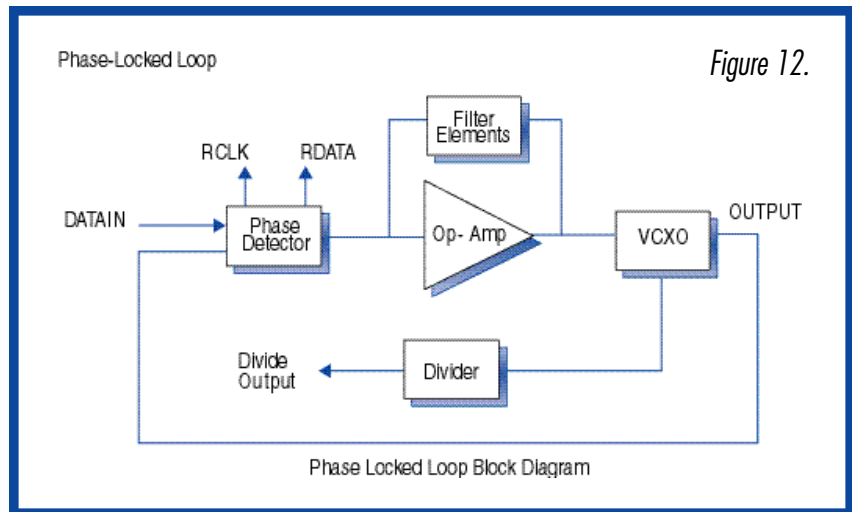


Figure 12.

A designer's primary concern is to select a loop filter that ensures lock-in and stability, while providing adequate filtering of input signal noise or jitter. An initial design starts with a known DATAIN signal and an output specification. An initial analysis of the open loop gain response provides insight into the response of the system.

Using Figure 12, the open loop gain is:
$$G(s) = \frac{K_p k_V A_V(s)}{sN}$$

Where:

K_p is the phase detector gain in V/rad (0.53 x Data Density or 0.35 x Data Density for 3.3V).

k_V is the VCXO gain constant in Rad/Vs.

$A_V(s)$ is the loop filter transfer function.

N is the divide ratio.

$1/s$ converts the VCXO frequency output to a phase output.

The open loop gain may be plotted and varied using the SPICE model provided in Figure 13. The gain, frequency, and loop filter configurations may be varied to produce desired responses. In the first-order phase-locked loop, where $A_V(s)$ and N equal 1, the gain curve has a 20 dB/decade slope with unity gain at:

$$f = \frac{k_V K_p}{2} \text{ where } k_V \text{ is in rad/Vs.}$$

The first-order open loop gain has a constant phase shift of 90 degrees. However, other frequency poles are present in the loop due to the op-amp's limited bandwidth and gain, the phase detector and the VCXO modulation bandwidth (these poles are included in the SPICE model). The loop's bandwidth is approximately equal to the closed loop bandwidth and can be used to assess the stability, lock-in range and filtering characteristics of the loop. The loop acts as a bandpass filter centered at the clock frequency, just as if a tank circuit were used to filter the input clock or data stream.

However, the filter Q of the CD-700 is much greater than that of a tank circuit and typically ranges from 1,000 to 20,000. The PLL tracks input phase jitter inside the loop bandwidth while jitter is attenuated outside the loop bandwidth. Converting the SPICE model (Figure 13) to a closed loop illustrates the jitter transfer function shown in Figure 15. In general, the PLL rapidly locks those signals with an initial frequency difference (relative to CLKIN) that is within the loop's bandwidth. Lock-in time is longer for lower bandwidth loops and may be degraded by jitter or by poor input duty cycle.

Simulated Results

The SPICE model just described can be used to determine the component values necessary to produce a desired loop filter bandwidth, its jitter transfer function and its open loop response for a given application. Alternatively, simulation results can be obtained using Vectron's "CD-700/TRU-050 Loop Filter Calculation" software. This software runs from DOS and will also provide the user with loop filter component values R1, RF and CF (see Figure 15) based on desired loop filter bandwidth, data type, data density, damping factor and data frequency. For assistance with your specific application, or to receive a copy of Vectron's "CD-700/TRU-050 Loop Filter Calculation" software, please contact Vectron's Application Engineering staff. The CD-700/TRU-050 Loop Filter software is also available in the "Applications" section of Vectron's website: www.vectron.com

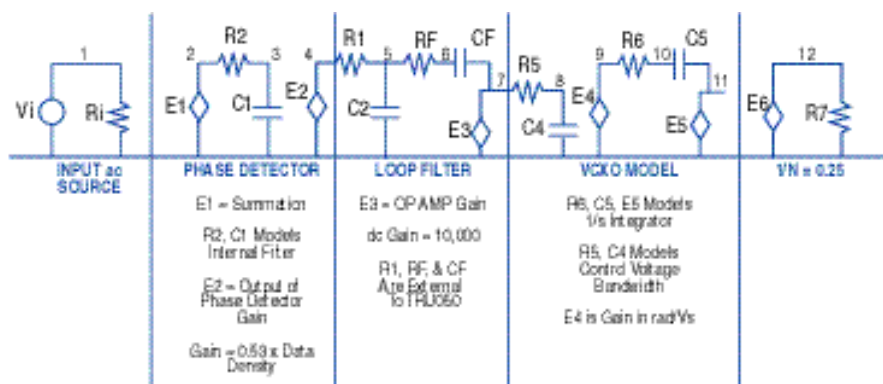


Figure 13.

SPICE Model

```
*****TRU050 ac Loop Model
vi 1 0 ac 1
ri 1 0 1k

*****Phase Detector
e1 2 0 1 0 1
(for closed loop response use:
e1 2 0 1 12 1)
r2 2 3 30k
c1 3 0 60p
*****Phase Detector Gain =
e2 4 0 3 0 0.XX
where 0.XX =
0.53 * Data Density for 5V
0.35 * Data Density for 3.3V
***

*****Loop Filter
r1 4 5 13.5k^1
c2 5 0 10p
rF 5 6 80k^1
cF 6 7 .1u^1
e3 7 0 5 0-10000

*****VCXO
*****Input Bandwidth = 50 kHz
r5 7 8 160k
c4 8 0 20p
*****VCXO Gain 2 Hz/V
*Example 100 ppm * f0 * 2 *
e4 9 0 8 0 20588

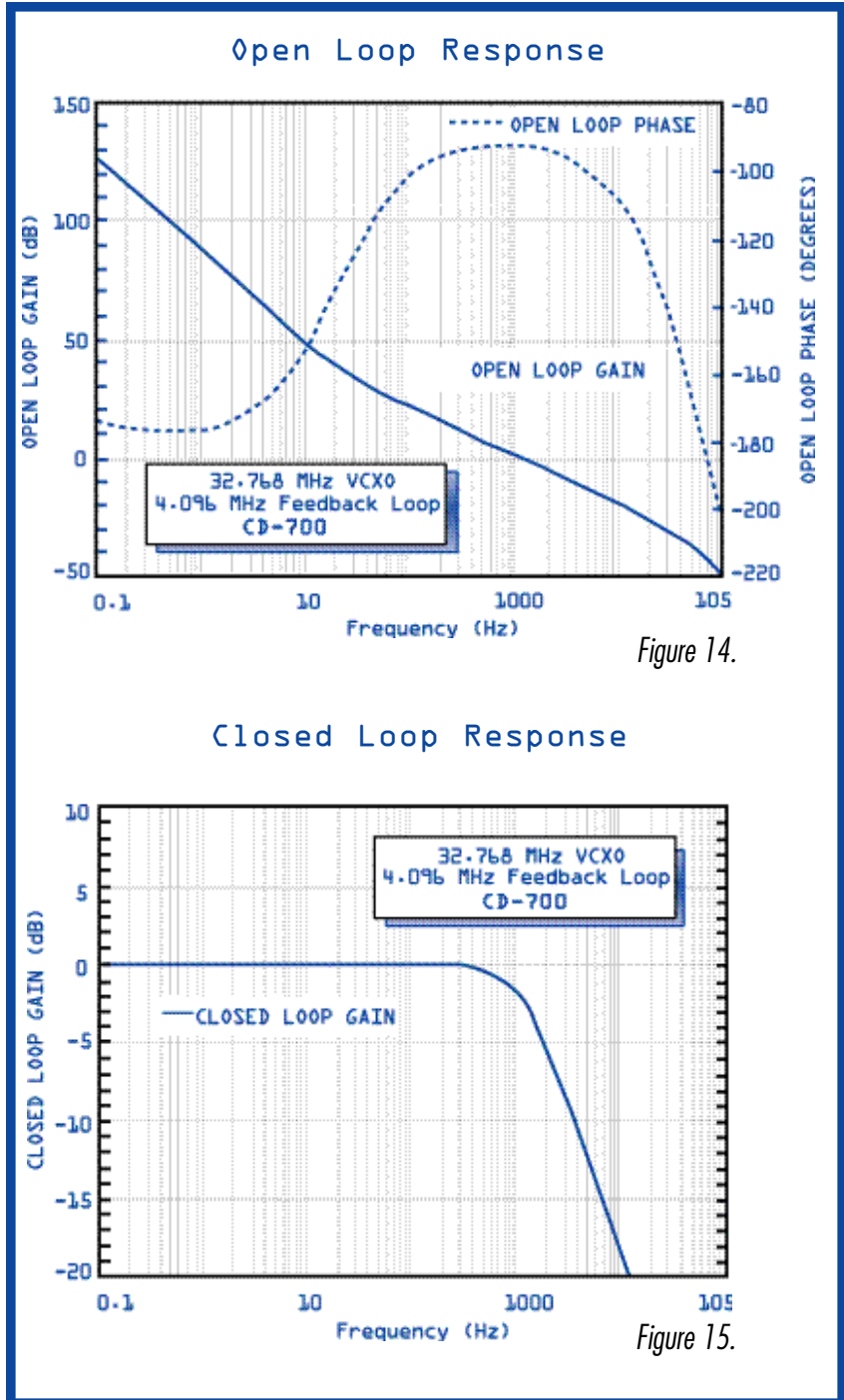
*****1/s Model
r6 9 10 1000
c5 10 11 .001
e5 11 0 10 0-1e6

*****Divide by N
e6 12 0 11 0 0.125^1
r8 12 0 1k
```

Note1: Defined by loopfilter and feed back gain

SPICE Simulated Results

- * Phase margin is 87.0 ° at 1000.0 Hz
- * Open loop gain margin is -3.92e+01 at 60000.0 Hz
- * Closed loop jitter bandwidth (-3 dB) is 1500 Hz.
- * The maximum value of the closed loop gain is 0.11614 dB at a frequency of 65.000 Hz
- * Damping factor = 4.0
- * $R1 = 13.5 \text{ k ohm}$
- * $Rf = 79.6 \text{ k ohm}$
- * $Cf = 0.10 \text{ } \mu F$
- * Data density = 100%
- * VCX0 FREQ = 32.768 MHz
- * Feedback divider = 8



How Is It Used?

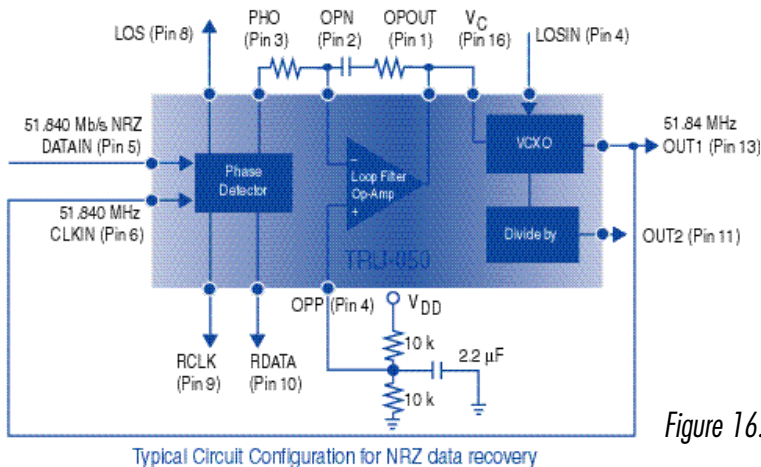
Applications

The three key applications for the CD-700 are clock recovery of digital data, frequency translation and clock smoothing. These timing needs are required by a wide variety of markets such as telecommunications, datacommunications, digital video and audio, telemetry, test equipment and sensing.

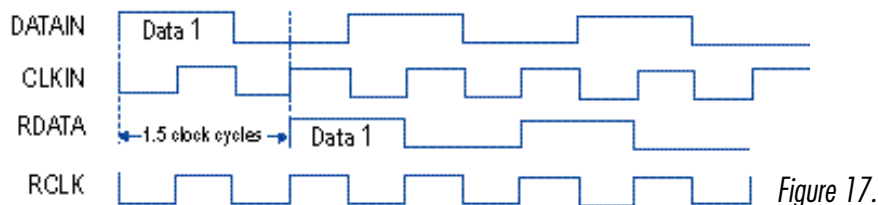
Clock Recovery and Data Retiming

The CD-700 was designed to recover a clock imbedded in an NRZ data signal, and retime it with a data pattern. In this application, the VCXO frequency is exactly the same as the NRZ data rate and the outputs are taken off Pin 9 (Recovered Clock) and Pin 10 (Recovered Data). The diagram below shows a typical circuit.

Figure 17 shows the relationship between DATAIN (Pin 5) and CLKIN (Pin 6) under locked conditions. The rising edge of the CLKIN is centered to the DATAIN pulse.

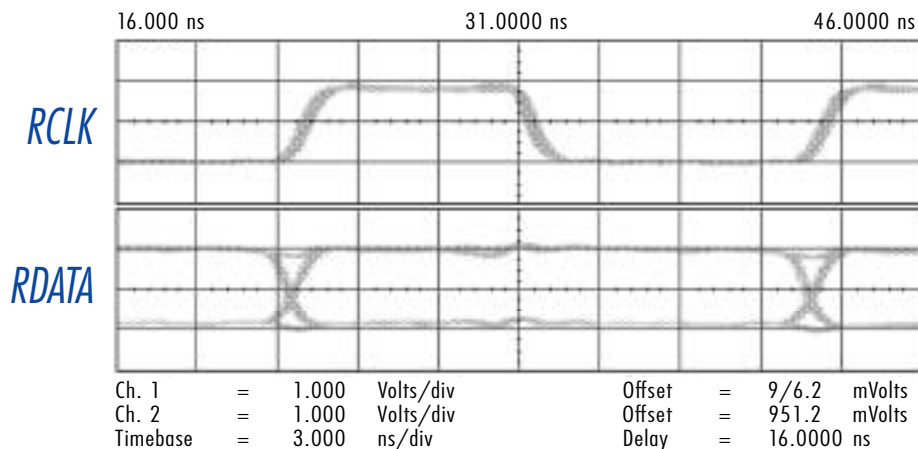


Relationship of RCLK (Pin 9) and RDATA (Pin 10). The falling edge of the Recovered Clock is in the middle of the data pattern and should be used to clock the data into the next part of the circuit. There is a one and a half cycle delay (frequency of Pin 6 between DATAIN and RDATA). Therefore a 10 MHz signal would have a 150 nS delay between DATAIN and RDATA plus additional circuit delays, which are typically 9 nS.



Is Vectron ISO registered?

Yes! Vectron's quality system was registered to ISO 9001 in October 1996.



Eye Diagram for
CD-700 @ 51.84 MHz

The falling edge of RCLK
is centered with respect
to RDATA

Figure 18.

Timing Recovery Using OUT2

Due to the limitations in crystal size, the lowest frequency from OUT1 is 12 MHz. For applications below this frequency, the internal divide-by can be used (Note: an additional external divide-by can also be used). An application for 1.544 MHz clock recovery is shown in Figure 19.

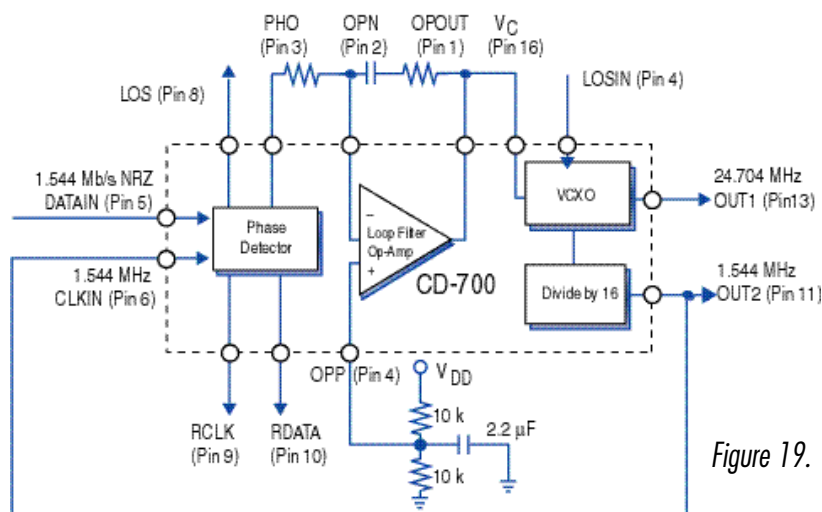


Figure 19.

Frequency Translation

The CD-700 is most commonly used for frequency translation. For example, in a telecommunications application, when a 2.048 MHz reference clock is multiplied to 32.768 MHz, a very clean 32.768 MHz clock would then be output to other circuits.

Generally, the CD-700 is specified in terms of NRZ input. Since the CD-700's phase detector was designed for NRZ data, other inputs such as a clock signal should be considered as an equivalent 1010...NRZ pattern.

If the DATAIN input to the phase detector is a clock signal, the VCXO, or the divided VCXO output fed back to CLKIN, must be twice the DATAIN rate. In Figure 20, the 2.048 MHz system reference clock can be treated as a 4.096 MHz NRZ data stream with a data density of 100%. Therefore, the feedback frequency in the PLL would be 4.096 MHz (the 32.768 MHz clock frequency divided by 8).

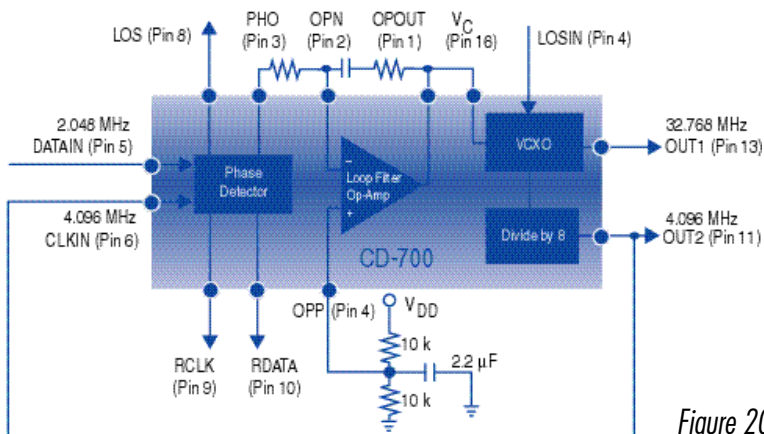


Figure 20.



The Timing diagram above shows a 2.048 MHz clock input being translated to 32.768 MHz clock output.

Figure 21.

Another example would be to translate 8.000 kHz to 51.840 MHz.

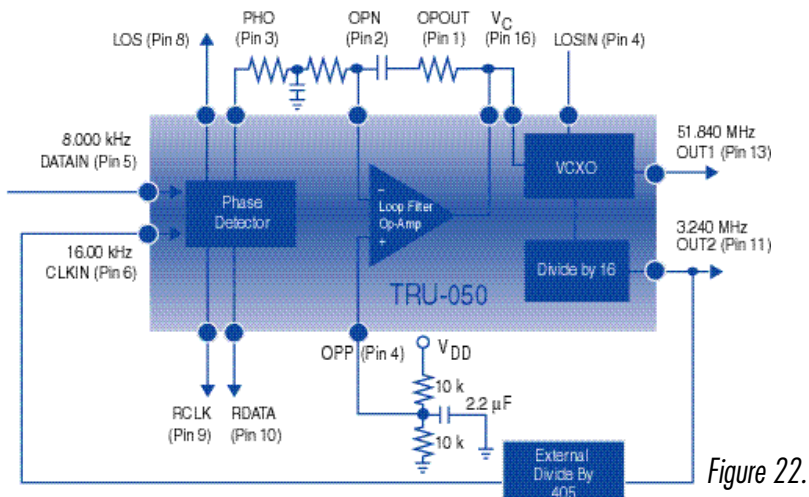


Figure 22.

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For applications where the DATAIN is very low in frequency (roughly <200 kHz), clock information may pass through the phase detector because of its finite low pass characteristics. In applications such as this, an additional pole may be necessary in the loop filter to attenuate these AC components prior to the VCXO input (note the capacitor to ground in Figure 22). Please contact Vectron's Applications Engineering staff for further detail.

Clock Smoothing Example

The third common application of the CD-700 is for the Regeneration or "Smoothing" of a degraded input clock signal. In this application, the CD-700 accepts a degraded input clock signal and regenerates the signal to square up the rising and falling edges and remove unwanted jitter. The output is then a clean quartz locked representation of the degraded input signal. Figure 23 illustrates a common example of a clock signal regeneration application. In this example, a degraded 16.384 MHz clock signal is smoothed using the CD-700. The 16.384 MHz clock is fed into DATAIN (Pin 5). The signal is then regenerated, and a smoothed representation of the signal is available at RDATA (Pin 10).

It is important to note that the signal fed back from OUT1 (Pin 13) to CLKIN (Pin 6) is twice the frequency of the degraded input signal at DATAIN (Pin 5). This is because the CD-700 was originally designed for input NRZ data patterns. Since an NRZ data pattern has one transition per bit, and its associated clock has two transitions per bit, the CD-700 phase detector requires twice as many transitions at CLKIN (Pin 6) when compared to DATAIN (Pin 5). In the case of an input clock signal, CLKIN (Pin 6) must be twice the frequency of DATAIN (Pin 5). For a 16.384 MHz clock smoothing application, a CD-700 with a 32.768 MHz OUT1 should be specified.

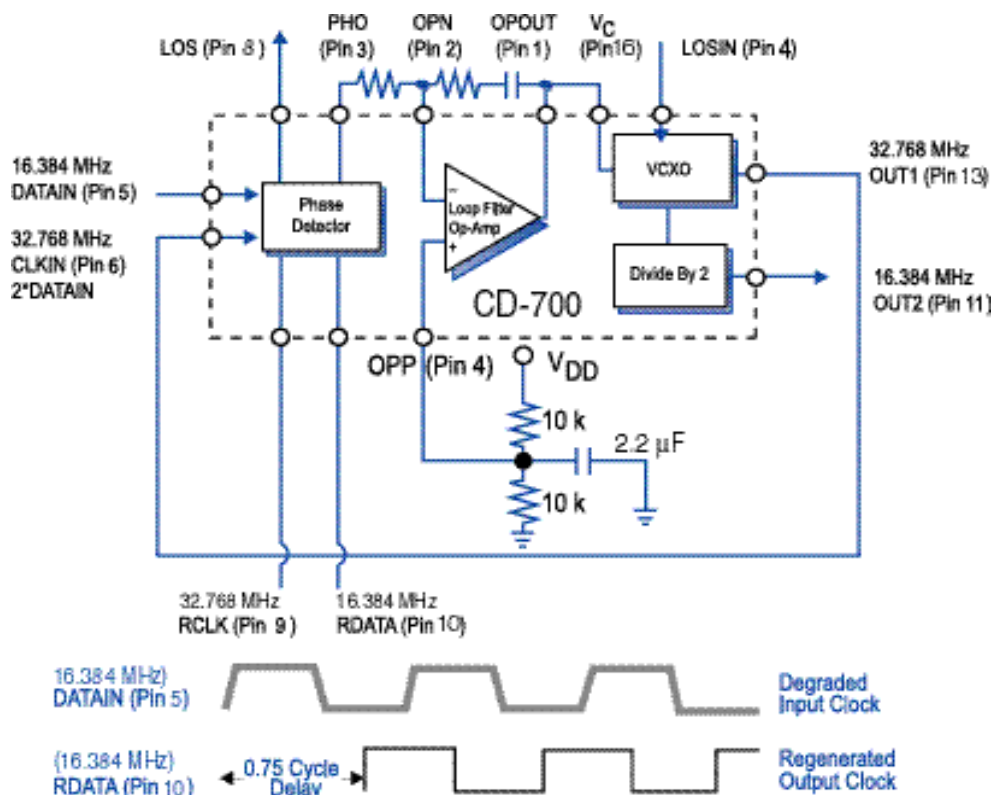
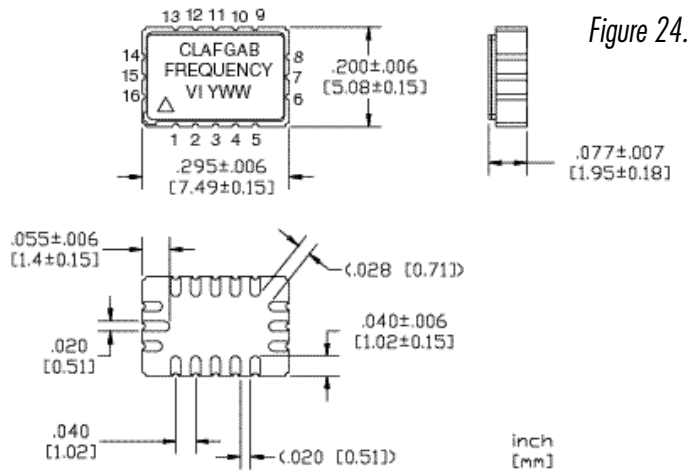


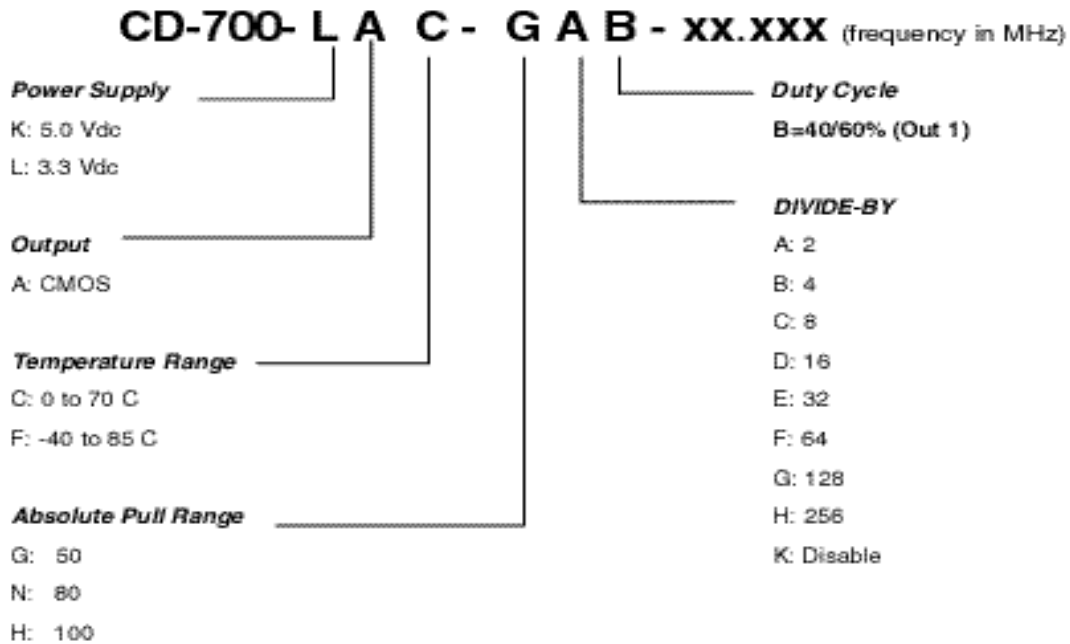
Figure 23.

How Is It Packaged?



Questions?
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How Is It Ordered?



Standard Frequencies* (MHz) Using OUT1														
12.000	12.288	12.624	13.000	16.000	16.128	16.384	16.777	16.896	17.920	18.432	18.936	19.440	20.000	20.480
22.1184	22.579	24.576	24.704	25.000	27.000	28.000	30.720	32.000	32.768	33.330	35.328	34.368	38.880	40.000
40.960	41.2416	41.943	44.736	47.457	49.152	49.408	50.000	51.840	54.000	60.000	61.440	62.208	62.500	65.536

*Other frequencies available upon request.

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